Millimeter-Wave Planar Log Periodic Antenna for On-Chip Wireless Interconnects

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***Abstract*—The performance of large multi-core chips have been limited by high power dissipation and latency problems associated with conventional interconnect topologies. On-chip wireless interconnect architectures with associated on-chip antennas have been recently investigated as a possible alternative to wired interconnects. In this paper, we propose the design for an on-chip planar log-periodic antenna with wide bandwidth and end-fire directivity at millimeter and/or microwave range of frequencies to improve the signal transmission characteristics of wireless interconnects. A two-port antenna network is simulated for 60GHz in HFSS and the radiation pattern and the scattering matrix parameters are presented.**

I. Introduction

Tens to hundreds of cores are integrated on a single die in modern multi-core chips. With the continuous decrease in device size and increase in number of cores, conventional interconnect lines are limited by associated high power dissipation issues, latency [1] and problems due to clock distribution networks [2]. This has led to research and development of alternate interconnect systems such as optical, 3D and/or RF [3] - [4], systems. These interconnects face limitations such as materials and process available for Optical Interconnect fabrication [5]. In recent years, microwave and millimeter wave wireless on-chip interconnection architectures have been investigated [6] - [9]. These wireless interconnects are CMOS compatible and do not require any new manufacturing technology. As a result, on-chip wireless interconnects looks most promising solution to be accepted by industry in near future among all other emerging interconnects. Several on-chip antenna designs such as loop, zig-zag, meander, linear etc [6] have been investigated. However, these antennas have omnidirectional radiation characteristics along the azimuth which result in poor utilization of the available frequency band. This also restricts the choice of network topologies that can be designed with on-chip wireless interconnects. This paper proposes to implement wireless interconnects with wide-band, end-fire directive antennas. These antennas allow the reuse of channel space and efficient utilization of wireless medium that were otherwise not possible with an omnidirectional antenna [10], [11].

Over several decades, planar log periodic antennas have been investigated for their ease of manufacture and for their wide-band properties [12]. However, to the best of the knowledge of the authors, these antennas have not been implemented on silicon substrates for wireless interconnects. In section II of this paper, we present a planar log-periodic on-chip antenna design that can be integrated with wireless interconnect architectures. The generalized design parameters allow the flexibility towards designing the antennas for specified frequencies. The antenna characteristics are simulated with finite element techniques on HFSS for 60GHz. The antenna shows 10% bandwidth and an end-fire directivity of 12.3 dB. In section III, we present different antenna characteristics such as return loss, azimuthal and elevation radiation pattern and transmission parameters in comparison with those of an on-chip patch antenna operating at same frequency.

II. Antenna Design

The main objective of this paper is to present a planar log-periodic antenna (PLPA) that can be integrated with wireless interconnection architectures at any specified frequency. Figure 1. shows the design of the antenna with eight teeth (marked 1 to 8) attached to an internal feed. The size of the teeth increase in a logarithmic manner as shown in table I. The

TABLE I
Dimensions of the antenna

Dimension	Length (mm)
L1	0.11000
L2	0.14019
L3	0.17867
L4	0.22772
L5	0.29023
L6	0.36990
L7	0.47144
L8	0.60085
L9	0.05500
W1	0.11000
W2	0.16500
Substrate Height	0.385

dimensions that are mentioned in the table are specifically for 60GHz. These dimensions can be scaled appropriately for

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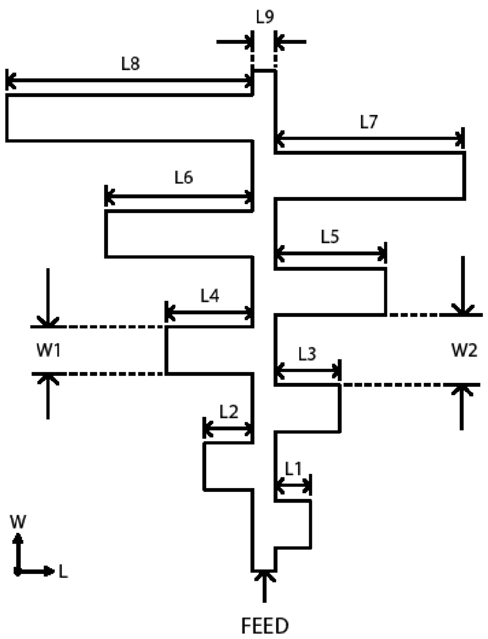

Fig. 1. On chip planar log-periodic antenna

any desired frequency of operation within the micro-wave and millimeter range. The longest dimension of the antenna is 1.1825 mm which is comparable to the wavelength of the signal in the dielectric medium, $\lambda_g = \lambda/\sqrt{\epsilon_r} = 1.14$m. Here, λ is the wavelength in free space and ϵ_r is the dielectric constant of a 10-20 Ω-cm silicon substrate which is commonly used in CMOS and BiCMOS technologies. The feasibility of this substrate has been previously studied by [13] - [15]. In the case of a 60 GHz antenna, the height of the silicon substrate is 0.385 mm and a layer of SiO_2 of thickness 0.0123 mm is placed over the substrate to provide some insulation between the antenna and the ground plane. The antenna which is of 0.055 mm thick conducting metal is placed on the SiO_2 layer as shown in Figure 2. A wireless interconnect can be

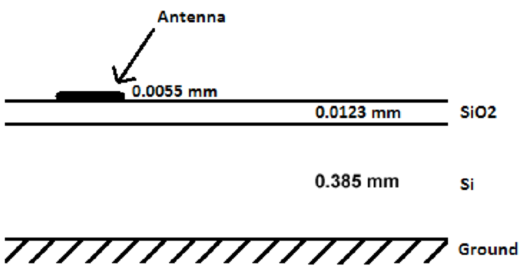

Fig. 2. Cross section of the antenna on the silicon substrate

implemented by establishing a communication link between antennas on the same substrate with one antenna in the end-fire region of another.

III. Simulation Results

The 60GHz on-chip PLPA described in Section II is simulated using FEM based HFSS software and the results are presented in this section. The return loss of the antenna i.e. S_{11} parameter is shown in Figure 3. The figure indicates that this antenna can be operated as a dual-band antenna at 44 GHz and 60 GHz with a bandwidth of 10% at 60GHz. The wide-band nature of the antenna can be attributed to the log-periodicity in the antenna design.

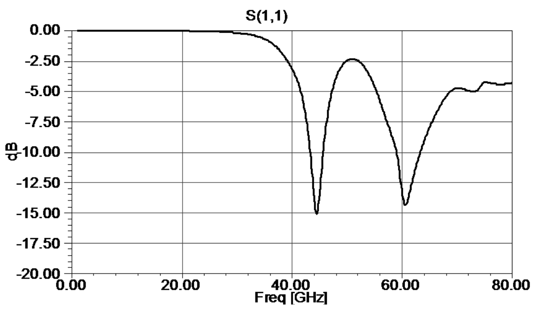

Fig. 3. Return loss of the on-chip planar log-periodic antenna

Figure 4, the radiation pattern of the antenna in the azimuth plane, clearly demonstrates the end-fire directivity of the antenna. The half-power beamwidth of the on-chip PLPA is 33° along the end-fire when compared to 100° of the patch antenna along the broad-side. Similarly, the half-power

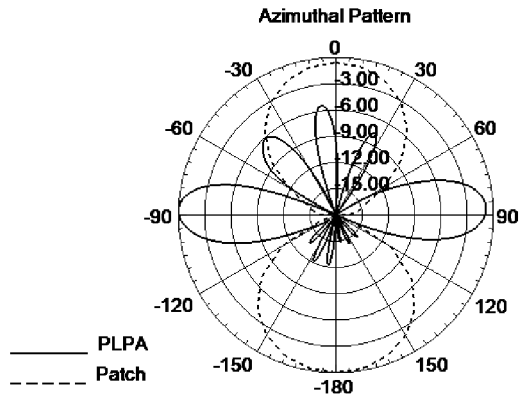

Fig. 4. Radiation pattern along the azimuthal plane

beamwidth along the elevation, shown in Figure 5, is 30° when compared to 108° corresponding to the patch antenna. Note the presence of large grating lobes which is characteristic of end-fire operations of linear arrays.

Next, we simulated the transmission characteristics of the two PLPAs integrated on the same substrate separated by a distance of 20mm. The antennas are aligned such that maximum signal can be coupled between the antennas. In other words, one antenna is oriented along the end-fire region of the second antenna. The transmission gain between the antennas is computed according to (1), where S_{11} = S_{22} since

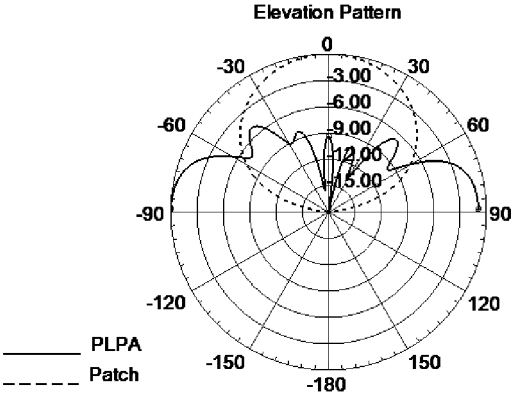

Fig. 5. Radiation pattern along the elevation plane

the we have same antenna on transmitting and receiving end.

$$G_a = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \tag{1}$$

The results are presented in Figure 6. At 60GHz, the gain is -38.65dB which is strong compared to the results reported in [6]. The improved performance is due to the increased end-fire directivity of the on-chip PLPAs. When the simulations were repeated for patch antennas on a similar substrate, the gain was very low and limited by the quantization error of the simulation.

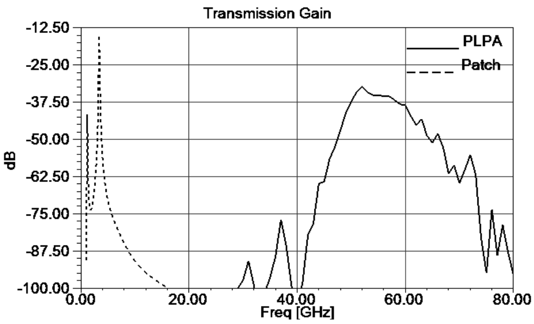

Fig. 6. Transmission gain between two on-chip antennas integrated on a common silicon substrate

IV. Conclusion

A planar log-periodic antenna on a silicon substrate has been proposed for on-chip wireless interconnects at millimeter wave frequencies. The antenna has a wide bandwidth of 10% and high end-fire directivity of 12.3 dB which makes it suitable for transmission of large data on a chip. However, the antenna is associated with large grating lobes typical of many end-fire antenna array configurations.

Acknowledgment

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References

[1] International Technology Roadmap for Semiconductors, 2011. Ch. - Interconnects.

[2] V. Mehrotra V, D. Boning, "Technology scaling impact of variation onclock skew and interconnect", IITC. San Francisco, CA: IITC;2001.

[3] DAB Miller, "Optical interconnects to silicon", IEEE J. Sel. Top. Quantum Electron 2002;6:13127

[4] S. J. Souri, K. Banerjee, A. Mehrotra, K.C. Saraswat, "Multiple Si Layer ICs: Motivation, performance analysis and design implications", Proceedings of the 37th ACM Design Automation Conference 2000, pp. 87380.

[5] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, and P. M. Fauchet, "On-chip optical interconnect roadmap: Challenges and critical directions," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 16991705, Nov./Dec. 2006

[6] K. K. O, K. Kim, B. A. Floyd, J. Mehta, H. Yoon, C. M. Hung, D. Bravo, T. Dickson, X. Guo, R. Li, N. Trichy, J. Caserta, W. Bomstad, J. Branch, D. J. Yang, J. Bohorquez, E. Seok, L. Gao, A. Sugavanam, J. J. Lin, J. Chen, and J. Brewer, "On-chip antennas in silicon ICs and their application", *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 13121323, Jul. 2005.

[7] B. A. Floyd, Chih-Ming Hung, and K. K. O, "Intra-Chip Wireless Interconnect for Clock Distribution Implemented With Integrated Antennas, Receivers, and Transmitters", *IEEE Journal of Solid-State Circuits*, Vol. 37, No.5, pp 543-552, May 2002.

[8] B. Moore, M. Margala, C. Backhouse, "Design of wireless onwafer submicron characterization system", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 13, No. 2, pp 169-180, Feb 2005.

[9] N. Miura, D. Mizoguchi, M. Inoue, T. Sakurai, T. Kuroda, "A 195-gb/s 1.2-W inductive inter-chip wireless superconnect with transmit power control scheme for 3-D-stacked system in a package", *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 1, pp. 23-34, Jan 2006.

[10] Amlan Ganguly, Kevin Chang, Sujay Deb, Partha Pande, Benjamin Belzer, Christof Teuscher, "Scalable Hybrid Wireless Network-on-Chip Architectures for Multi-Core Systems", *IEEE Transactions on Computers (TC)*, Vol. 60, Issue 10, 2011, pp. 1485-1502.

[11] Sujay Deb, Kevin Chang, Amlan Ganguly, Xinmin Yu, Partha Pande, Deuk Heo, Benjamin Belzer, "Design of an Energy Efficient CMOS Compatible NoC Architecture With mm-wave Wireless Interconnects", *IEEE Transactions on Computers (TC)*, DOI: 10.1109/TC.2012.224.

[12] Z. N. Chen, M. J. Ammann, X. Qing, X. H. Wu, T. S. P. See, and A. Cai, "Planar antennas," *IEEE Microw. Mag.*, vol. 7, no. 6, pp. 6373,Dec. 2006.

[13] K. Kim and K. K. O, "Characteristics of integrated dipole antennas on bulk, SOI, and SOS substrates for wireless communication", in *Proc. Int. Interconnect Conf.*, Jun. 1998, pp. 2123.

[14] K. Kim, H. Yoon, and K. K. O, "On-chip wireless interconnection with integrated antennas", in *IEDM Tech. Dig.* , Dec. 2000, pp. 485488.

[15] J. J. Lin, L. Gao, A. Sugavanam, X. Guo, R. Li, J. E. Brewer, and K. K. O, "Integrated antennas on silicon substrates for communication over free space", *IEEE Electron Device Lett.*, Vol. 25, No. 4, pp. 196198, Apr. 2004.