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Millimeter wave wireless interconnects in deep submicron chips: Challenges and opportunities

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ABSTRACT

On-chip wireless links offer the most promising solution to improve performance over traditional Networks-on-Chip (NoCs). Though, significant advancements are being made to support intra-chip wireless communication, a complete understanding of on-chip wireless channel, that facilitates design optimization of transceivers and antennas is still lacking. In this work, we derive on-chip wireless channel characteristics, taking into account antenna implementation, near field and multipath propagation effects. These observations are then used to study impact on wireless NoC performance, packet energy, delay and bandwidth. The study provides crucial insights for circuit designers to tune transceiver and antenna specifications to achieve desired network performance.

1. Introduction

With increase in integration levels of silicon technologies and paradigm shift towards multi-core designs, manifold increase in number of cores on a single die is anticipated over next few years. Network-on-Chip (NoC) platforms, for these Multi-Processor Systems-on-Chip (MPSoCs) play a crucial role towards sustaining the expected growth of computing performance. Existing NoCs with planar metal interconnects, are limited by high latency and power consumption of multi-hop wired links for long distance communication across the chip. Improving characteristics of metal wires does not satisfy network performance requirements in the long term, and new interconnect paradigms are needed to meet communication needs of MPSoCs. To this end, novel approaches like 3D integration, optical interconnects, RF interconnects (RF-I) and wireless interconnects with millimeter (mm-) wave antennas have been proposed. Of these, mm-wave wireless interconnects offer the most feasible solution because of their compatibility with existing manufacturing processes and ease of integration without requiring significant new technological innovations or compromises. Besides this, on-chip wireless links are also more suitable for broadcast messages that are fairly common in multi core systems. Studies on Wireless NoC (WNoC) suggest that they provide enhancement in NoC performance by augmenting existing network through low latency and low energy long range wireless links [1,2]. Though these works highlight several advantages of using wireless links in NoC architectures, it is important to note that these analyses are not based on physical implementations of on-chip wireless links. Most analyses make the fundamental assumption that signal transmission through on-chip wireless channel resembles that of free space (Air/Vacuum).

There have been several endeavors to design and implement efficient on-chip antennas and circuitry for wireless links in WNoCs. On-chip integrated antennas for intra chip wireless communication operating in 10's to 100's GHz have been implemented in Refs. [3–6]. A fully integrated phased array antenna and transceiver design for on-chip wireless links operating at 77 GHz have been presented in Refs. [7,8]. A comprehensive overview of on-chip antennas, their implementation, benefits and challenges is presented in Ref. [9]. Simultaneously, there have been studies on the effects of substrate properties and simple geometries on the characteristics and performance of integrated antennas for intra chip wireless communication. Authors of [10] have investigated intra-chip communication at sub-mm frequencies and shown the feasibility of on-chip wireless communication. Authors of [11] have studied the effect of silicon substrates on integrated antennas and found that gain can be improved by using high resistivity silicon substrate. Authors of [12,13] have provided guidelines to improve on-chip antenna characteristics in presence of metal interference structures. An analysis of antenna efficiency under different configurations of silicon substrate and ground shield has been presented in Ref. [8]. Besides these, a few works have also analyzed the behavior of signal propagation in intra chip wireless channel. Authors of [14], by studying propagation mechanisms in intra chip channels, have shown that path loss factor and propagation delay vary significantly from free space transmission. A study in Ref. [15]

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Table 1
Summary of existing and proposed works for on-chip wireless link analysis.

Ref	Analysis Approach	Intra Chip Setup	Intra Chip Components	Objectives	Results
[7,8]	Simulation/ Measurement	2D	Si substrate, SiO_2 dielectric, ground plane	Antenna/Transceiver design	Ground shield above substrate with sufficient distance improves transmission, various substrate and ground shield setups
[10, 11]	Measurement	3D	Bulk + Oxide layer, backplane	Antenna performance on different substrates	Radiation in on-chip environment is feasible
[12, 13]	Measurement/ Simulation	3D	3 metal layer CMOS chip	Antenna performance analysis and design rules	Avoid metal structures above and parallel to antennas
[14]	Measurement	3D	Si substrate, SiO_2 dielectric	Frequency and time domain analysis of intra chip channel	Significantly high propagation delay, surface wave propagation, metal lines in parallel or normal improve surface transmission
[15]	Simulation	2D	Si substrate, SiO_2 dielectric	Theoretical analysis of intra chip wave propagation using Green's functions	Surface wave may not be dominant, guiding layer below substrate improves surface wave
This	Simulation	3D	9 metal layer CMOS chip	Detailed understanding of on-chip wireless channel and design guidelines at all levels	Includes near field effects, antenna over cavity, high delay spread, path loss and propagation delay, design guidelines

has used a Green's function-based channel model to establish different propagation paths between on-chip wireless transmitter and receiver. However, their research was confined to simple substrate geometries that did not include metal interconnects and other propagation effects. Multiple metal layer stacks in Deep Sub-Micron (DSM) technology and intricate chip geometries have severe implications on on-chip wireless channel resulting in channel fading, dispersion, etc. Proximity of integrated antennas to wired metal interconnects degrades their efficiency significantly, thereby increasing antennas loss and transmission power. Additionally, wireless transmission in intra chip environments is predominantly in near field propagation region, limiting the use of classical analysis based on antenna gain, directivity, etc. which assume far field constraints. None of the existing works thoroughly examine these limitations imposed by DSM technology design parameters and complex intra chip geometries on wireless channel and signal propagation characteristics, that can have significant impact on circuit design, network and system performance.

In order to facilitate the efficient design of on-chip wireless communication infrastructure, there is a fundamental need to establish detailed wireless channel characteristics for CMOS design parameters. The objective of our work is to provide a comprehensive and detailed analysis of on-chip wireless channel including the effects of silicon bulk substrate, silicon-di-oxide, metal interconnect stack and their configuration. Using on-chip wireless channel analysis, we derive channel characteristics like path loss, delay spread, propagation delay and their inter-dependencies, which can then be used to obtain a realistic estimate of wireless link performance in WNoCs. We also propose design changes for implementation of integrated antennas in CMOS chips for improved efficiency. The study can provide crucial insights to system designers to optimize design parameters for antennas, transceivers and network topologies on the basis of underlying channel propagation.

To achieve a detailed understanding of signal propagation characteristics in on-chip wireless channel with near field and multipath propagation effects, we develop a three-dimension model of the complex chip geometries with metal interference structures. We employ transient domain-based solvers to simulate electromagnetic propagation between two antennas in these intra chip environments and study channel propagation physics. Table 1 summarizes the existing works and proposed work for intra chip wireless channel analysis in terms of their setup, objectives and findings. While works presented in Refs. [10–13] have included full metal layer stack of CMOS chip, their objective is analyzing and to improve antenna performance. On the other hand, propagation analysis in Ref. [15] provides insights into channel characteristics, but models the chip as 2D multilayered structure without metal layer stack. To the best of our knowledge, analysis in Ref. [14] includes detailed insights into channel performance through measurements of fabricated antennas on Si substrate and SiO_2 layers and also includes study of impact of metal interference structures on channel characteristics. In contrast, we model the full metal layer stack of CMOS chips, place the antenna in top metal and understand channel propagation within this setup through electromagnetic simulations.

The antennas are excited by a Gaussian source with bandwidth in unlicensed mm-wave frequency range of 55–65 GHz. The operating frequency is chosen in mm-wave frequency range because of the compatibility of mm-wave antennas with CMOS manufacturing process. We analyze the received field at different distances from transmitting antenna and obtain channel path loss, delay spread and propagation delay. We estimate the path loss decay rate, delay spread and propagation delay as functions of the distance between the transmitter and receiver antennas. We also analyze the impact of silicon-di-oxide layer thickness and proximity of antenna to metal interconnects in these geometries on antenna characteristics like return loss, bandwidth, etc. These analyses are then used to establish guidelines for antenna structures, their placement and to compute transmission power requirements and signal data rate of wireless interconnects for tuning underlying analog circuit design parameters. We present an illustration of channel impacts on delay and energy using wireless links for on-chip data transmission and compare the values with that of free space channel values. The major contributions of this work are:

1. Study of intra chip geometries for wireless propagation and challenges for estimation of channel characteristics.
2. A detailed multi-layered three dimensional model for intra chip wireless channel, including substrate, metal layer stack, dielectric layers, etc.
3. A novel way of implementing on-chip antennas for improving its return loss and bandwidth in presence of metal layer stack.
4. Analysis and computation of path loss, delay spread and propagation delay with distance from transmitting antenna in intra chip wireless channel.
5. Guidelines for implementing on-chip wireless links and brief analysis of the impact of wireless channel characteristics on network performance and energy.

Our paper is organized as follows. In the following section, we present brief overview channel estimation challenges and its impact on link performance and efficient circuit design. The proposed 3D model of multi-layered on-chip environment is discussed in section 3. In section 4, we analyze the transmitted signal characteristics and derive on-chip wireless channel properties and provide guidelines for enhancing wireless interconnect performance. Using this analysis, we provide design guidelines for WNoCs from antenna implementation, circuit to system level in section 5. We provide a brief analysis of impact of intra chip wireless channel on WNoC performance in section 6. Finally, we

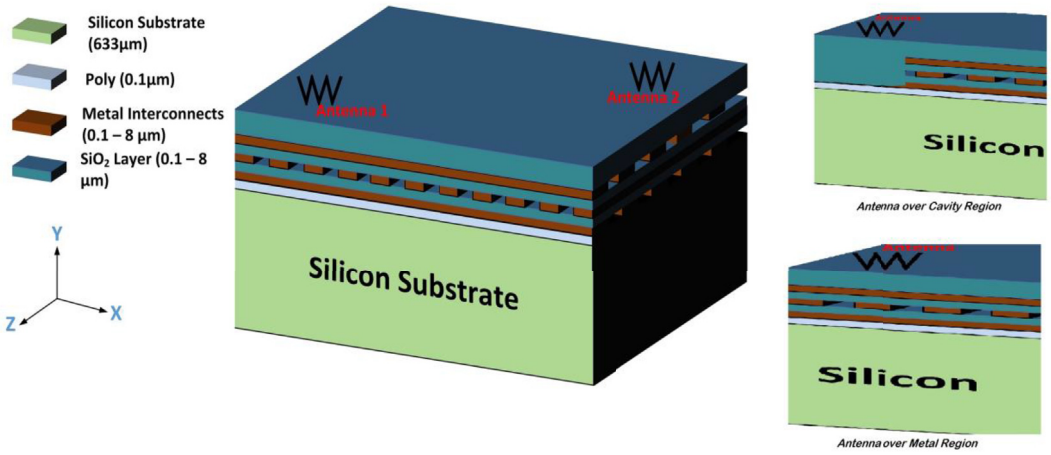


Fig. 1. 3D on-chip environment with a silicon substrate, copper interconnects and silicon-di-oxide for wireless channel estimation.

summarize our findings in section 7.

2. Wireless channel estimation and link performance: challenges

Data communication using wireless links is dependent on efficient design of transceiver and antenna and signal transmission through wireless channel. Key design choices of transceiver like input transmission power, signal data rate, amplifier sensitivity, along with link latency and loss performance are heavily influenced by wireless channel characteristics. Hence, it is imperative to obtain a comprehensive understanding of on-chip wireless channel for accurate analysis of wireless network performance and optimal tuning of transceiver specifications. Wireless channel, comprised of any and all components between source and receiver antennas, may alter signal path, reduce its power, induce noise, etc. and channel estimation includes analysis of all such effects. On-chip wireless channel, with its complex geometries and materials of different properties, poses many significant challenges for efficient estimation of its characteristics. We, first present a brief of overview of on-chip wireless channel, challenges for estimation and our approach to analyzing intra chip wireless channel and its impact on WNoC performance.

2.1. Intra chip geometries

On-chip wireless channel, unlike most classical wireless environments, is much more complex due to the intricate geometries formed by billions of transistors and their interconnections within the chip. Major components that comprise the wireless channel include bulk substrate generally comprised of silicon, silicon-di-oxide used as dielectric/insulating material and copper metal for wired interconnections. The elaborate shapes, different material properties, dimensions varying from nm to mm make wireless channel very complex, deviating link characteristics significantly from simple free space estimates. It makes wireless channel modelling and accurate estimation of performance significantly challenging.

2.2. Near field effects

Another fundamental challenge to channel estimation in WNoCs is that wireless propagation between two antennas is in near field/transition region as opposed to far field in more classical setups. Far field constraint for electrically short antennas (largest antenna dimension less than $\lambda/2$) puts minimum transmitting distance between antennas at $r \gg 3\lambda$ [16]. For mm-wave WNoCs, minimum transmission distance between antennas must be much larger than 15 mm. With on-chip wireless propagation distances typically varying from 5 mm to 25 mm and multiple antennas in close proximity, intra chip wireless transmission is dominantly in near field region. Unlike far field region, the electric and magnetic fields and their relationship is not well defined in the near field region. This prevents use of traditional loss and delay estimates for on-chip wireless channel estimates. In our analysis, we compute the channel characteristics from the simulated electric and magnetic field at each point in the channel. To be strictly in far field range, antennas operating in sub-THz or THz frequency range are required, which are achievable with Carbon NanoTube (CNT) and require significant changes to CMOS manufacturing process. The analysis of intra chip channel at these frequencies is beyond the scope of this paper and is reserved for our future work.

2.3. Multipath propagation

The complex geometry of intra chip environment, as de-scribed, leads to many different propagation paths in on-chip wireless transmission. Besides the line-of-sight component between antennas, transmitted signal can find different paths due to reflections from (a) multiple layers stacked along height of the chip and (b) chip edges in the antenna plane. Along the height, major propagation paths include reflected components from the interfaces of silicon substrate, metal layers, SiO_2 dielectric medium and free space within the chip. The paths traveled by reflected components vary depending on relative position of the antennas. Different components experience different path loss, propagation delay, and interference from other reflected components, resulting in huge variations in both signal strength and delay at the receiver. This complicates tuning of transceiver parameters for each setup or tuning the design to worst case scenarios leading to underutilized resources. Multipath propagation also makes the channel dispersive and distorts signal shape, requiring reshaping circuits to compensate for delay spread and distortion. This increases design area and power overheads.

2.4. Channel estimation

The intricate chip geometries, near field and multipath effects render traditional free space estimates ineffective for on-chip wireless links and performance evaluation of WNoCs. Without reliable information of wireless channel characteristics, design of antennas, transceivers, and network topologies to achieve desired performance is a challenging task. To overcome these challenges and obtain reliable estimate of wireless link properties, we develop a multi-layered three-dimensional model of intra chip environment to analyze wireless signal propagation between transmitter and receiver antennas. Transient domain, Finite Domain Time Difference (FDTD) technique, often useful for analyzing complex electromagnetic problems, is used to study signal propagation. Channel

Table 2
Material properties and dimensions of the on-chip propagation environment model.

Layer	Dielectric Constant	Conductivity (S/m)	Thickness (μm)
Silicon (Bulk)	11.9	2.5×10^{-4}	633
Metal Interconnects	–	5.8×10^{7}	0.1–8 (increasing from M1 to M9)
SiO_2 Layer	3.9	10^{-10}	0.1–8
Top Dielectric Layer	3.9	10^{-10}	25

characteristics like path loss, propagation delay, and delay spread are derived from observed results. We, then utilize this analysis to obtain design guidelines and realistic estimates of wireless link and WNoC system performance. We use antennas with different radiation patterns to study different propagation paths and their impact on loss and delay spread. The established channel characteristics are applicable to most existing chip setups and wide range of antenna designs. This allows circuit designers to implement underlying analog and digital logic to work with any design and achieve optimal performance. Once the desired components are chosen, the final characteristics can be obtained by combining channel and circuit properties. The study provides crucial insights into the on-chip wireless propagation characteristics and provides an abstraction of physical link model to be used by circuit designers for tuning the parameters to achieve required efficiency.

3. On-chip model and simulation setup for channel estimation

To analyze wireless transmission between antennas and estimate on-chip wireless channel, we model the intra chip environment using 3D multi-layered structure.

3.1. 3D on-chip model

The 3D model, shown in Fig. 1 captures all key parameters that influence wireless channel characteristics. The model consists of multiple layers with each layer rep-resenting different components of a DSM chip. The layers are stacked along Y-dimension with each layer spanning XZ plane. The devices (transistors, passive components etc.) are fabricated on a silicon substrate. Since transistor device dimensions are of the order of nano-meters and substrate thickness runs into hundreds of micrometers, we model them as a single homogeneous layer made of silicon, represented as Silicon Substrate in Fig. 1. The narrow Poly layer above silicon substrate is representative of polysilicon used for gate contact in CMOS process. The multiple layers on top of the silicon substrate and poly constitute the different metallic interconnects embedded within SiO_2 material. These interconnects, connecting different devices, span different lengths and are oriented in different directions (X and Z) and are interspersed by SiO_2. We consider the nine-metal layer process (M1 - M9) from 32 nm technology and dimensions for each layer are obtained from Ref. [17] (Fig. 1 is illustrative and does not show all nine metal layers). Metal interconnects in two subsequent layers are separated by SiO_2 material. In each layer, multiple interconnects of different lengths run parallel to each other; with any two interconnects in the same layer separated by spacing determined by the pitch of that layer [17]. The silicon substrate, poly and metal layers interspersed within SiO_2 represent the conventional chip components in any IC.

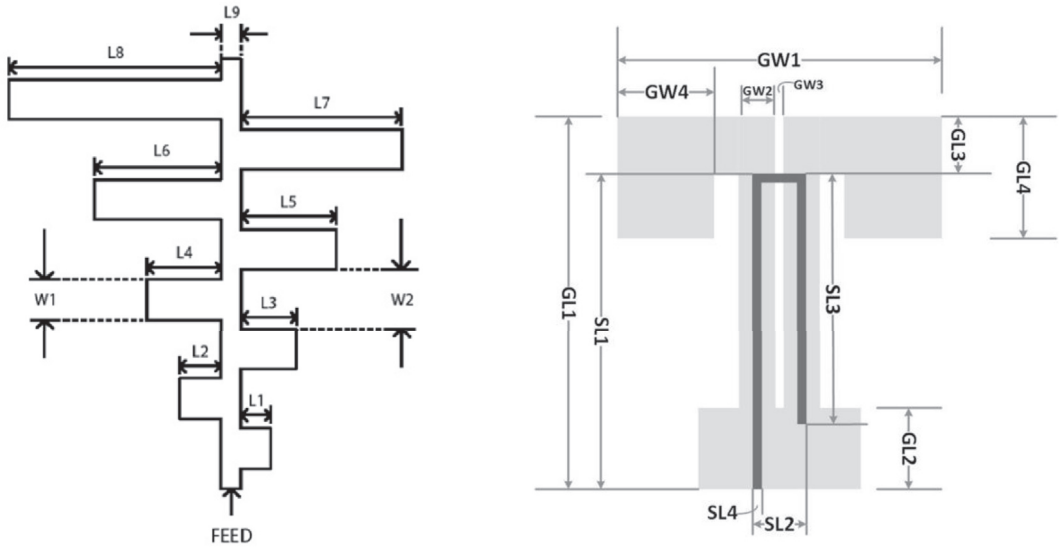
In on-chip antenna fabrications, typically, antenna is etched in the top metal layer as shown in Fig. 1 to reduce the interference from wired interconnects in the IC. Analysis of metal interference structures on antenna performance in Refs. [12,13] shows that metal interference structures above the antenna severely impact the gain and S_{11} and have to be avoided. Hence, in all our simulations, we place the antenna in the top metal layer as shown in Fig. 1. We further propose a novel way to implement on-chip antennas for improving their efficiency in presence of wired interconnects, discussed in detail in section 3.2. The antennas and top of model are exposed to free space, representative of vacuum inside the chip. The total 3D propagation model is bounded by Perfectly Matched Layer (PML) [18] bounding region with free space properties to prevent reflections from boundaries of the simulated region. The dimensions and material properties of different layers in 3D chip model are specified in Table 2. Here, we ignore the effects of chip packaging because, in most cases, the spacing between the top layer and packaging is significantly higher (of the order of a few millimeters) than the thicknesses of other layers.

3.2. Implementation of on-chip antennas

Integrated antennas in on-chip environments experience interference from metal interference structures of wired interconnects used for data communication in MPSoC ICs. Design guidelines in Refs. [12,13] have proposed to avoid metal interference structures above the antenna. Following this, antennas in all our simulation setups are implemented in the top metal layer. To improve the efficiency of antennas in intra chip environments, we propose modifications to existing layer dimensions and a novel way to implement the antenna. Firstly, to reduce the impact of wired links, the thickness of SiO_2 layer between antennas and immediate lower metal layer (referred to as top dielectric layer) is increased. The top dielectric layer has thickness, that does not exceed 10 μm ($\approx\lambda/500$ for 55–65 GHz frequencies) in today's manufacturing technologies. This significantly reduces radiation resistance of antenna due to its proximity to metal layer and impacts its efficiency. We have varied the top dielectric layer thickness from 8 μm [17] to 40 μm and empirically 25 μm thickness provides the best performance without adding considerable modifications. While this improves the antenna efficiency, interference from metal structures in same layer still poses challenges to efficiency. Furthermore, increasing thickness of top dielectric layer also increases the via thickness and manufacturing complexity.

To improve the efficiency of antenna in practical intra chip environments, we propose a novel implementation to place the antenna over a cavity region formed in between the interconnect layers. This cavity region is completely filled with dielectric material, SiO_2 (generally used material in CMOS manufacturing processes) and no metal structures are allowed within this region. The lateral dimensions of the cavity region in XZ plane are chosen to offset the proximity of any other metal structures by a predefined distance (empirically evaluated to be 100 μm). This reduces the of antenna proximity to all other metal interference structures and improves its gain, S_{11} and bandwidth efficiency. To minimize the impact of cavity region on wired links and their routing, it is formed only in between metal layers M4 and M8 (empirically chosen). In addition, placement of antennas can be chosen to minimize the impact on interconnect routing due to cavity formation. Since, the entire cavity region is comprised of dielectric material, the proposed implementation does not impact vias or contacts between metal layers.

To show the improvements achieved by using cavity region, we model the placement of antenna and interconnect layers in Fig. 1 using three different configurations. In the first configuration, we use the previously analyzed setups, where antenna is placed atop silicon substrate and a layer of SiO_2. This configuration does not contain any metal layers and is referred to as *No Metal Interconnects* configuration. In second configuration, the antenna is etched in top metal layer; with interconnect layer stack *M1-M8* configured as existing in practical chip environments, shown in Fig. 1. We refer to this setup as *Antenna over Metal Region* and is as shown in Fig. 1. In the third configuration, we use the proposed implementation; wherever the antenna is to be placed, a cavity region filled with only SiO_2 dielectric medium is created within the interconnect layer stack. The antenna is placed over this cavity region and antenna performance is improved since the proximity to metal interconnects is reduced. We refer to this as *Antenna over Cavity Region* and is represented in Fig. 1.



(a) Planar Log Periodic Antenna (PLPA) (b) On-Chip Folded Dipole Antenna

Fig. 2. On-chip antenna structures simulated.

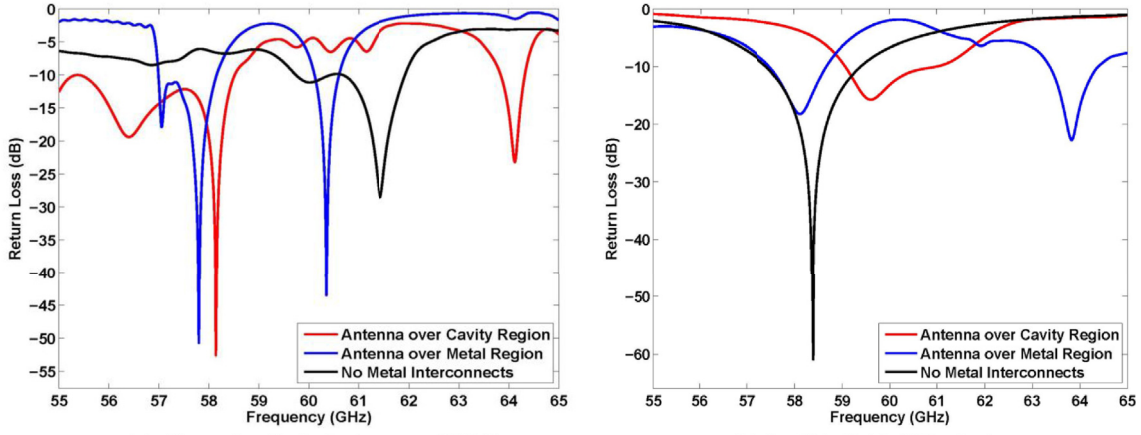
3.3. Simulation methodology

As described in section 2, wireless channel estimation in intra chip environments faces several challenges due to complex geometries, propagation in near field region and multipath effects. The sheer number of different on-chip components and several reflections from different layers and chip edges make development of closed form expressions for channel parameters a daunting task. Near field effects further adds challenges to theoretical analysis and efficient estimation of the channel.

To obtain channel characteristics in presence of near field and multipath effects, we simulate the signal propagation between two antennas in the proposed 3D chip model using Finite Differences Time Domain (FDTD) method. Signal propagation in near field/transition region does not have well-defined electric and magnetic fields and their inter relationship. Hence, we measure the individual field components at each point within the three dimensional multi layered model. The channel characteristics like path loss and delay are then computed from the received field components at different distances from the transmitting antenna. In addition to accounting for near field effects, the field measurement at any point includes all reflected components and constructive or destructive interference among them. This provides for accurate estimation of intra chip wireless channel characteristics.

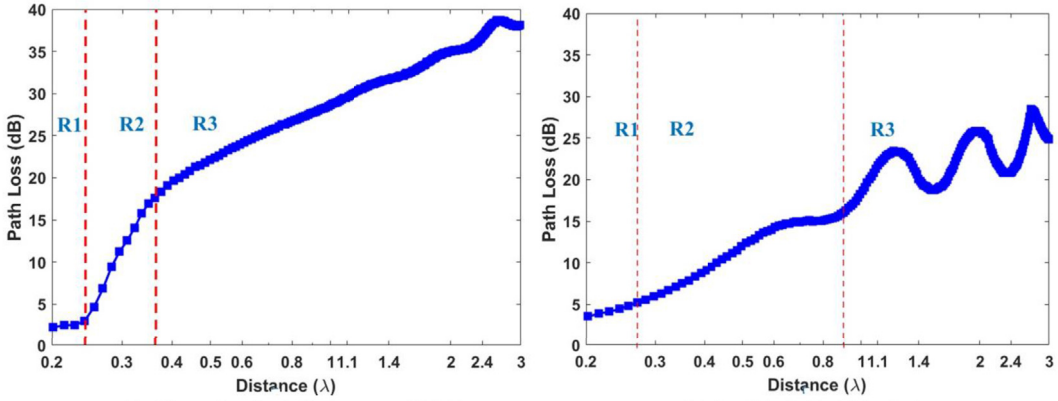
Furthermore, to demonstrate and understand multipath effects in detail, we use antennas with differing radiation directivities and thereby signal radiated in each direction. For this purpose, two antennas; folded dipole antenna [3] and Planar Log Periodic Antenna (PLPA) [4], shown in Fig. 2, are used for our simulations. Folded dipole antenna has a near omnidirectional radiation pattern while PLPA has directional pattern. Directional antennas, that radiate only in specific direction, potentially reduce the number of reflections and amount of signal coupled into different layers, thereby reducing impact of multipath propagation effects. Using the analysis with both antennas, we establish trade-offs between using any of the antenna types and their impact on channel characteristics and ultimately on circuit design and performance. Given the properties of antenna and nature of its radiation, end-to-end signal transmission using on-chip wireless links can be analyzed using the characteristics abstracted from channel estimation.

Finally, the propagation analysis is performed at mm-wave frequencies by exciting the transmitting antennas with a Gaussian pulse covering the frequency range of 55–65 GHz. The frequency band is chosen because the dimensions of the antennas radiating within this frequency range can be easily etched on top metal layer in existing CMOS processes. The estimation of channel characteristics at sub-THz and THz frequencies is reserved for our future work. Using this setup, the received



(a) Planar Log Periodic Antenna (PLPA) (b) On-Chip Folded Dipole Antenna

Fig. 3. Return loss in three dimensional on-chip environment for different configurations.



(a) Planar Log Periodic Antenna (PLPA) (b) On-Chip Folded Dipole Antenna

Fig. 4. Variation of path loss with distance from transmitting antenna.

signal at various distances and for different antenna configurations is analyzed to study impact of chip components, near field and multipath propagation effects. We derive path loss, propagation delay and dispersion of on-chip wireless channel at desired mm-wave frequencies. The estimated channel properties are then used to evaluate wireless links and network performance. Based on observed effects, we identify efficient ways to circuit implementation and trade-offs between different performance metrics.

4. Experimental results and observations

In this section, we discuss the analysis of on-chip wireless channel, its characteristics and how intra chip components effect the properties of channel. We provide design guidelines based on wireless channel analysis and study its impact on system performance. The three-dimensional chip model and wireless signal propagation between antennas is simulated using transient solver from CST MicroWave Studio (MWS) [19], which is based on FDTD techniques. The receiver antenna, at any distance, is placed in the end-fire radiation region of the transmitting antenna. The distance measured is from port to port of both the antennas. We consider distance between antenna ranging up to 20 mm which covers most on-chip long range wireless links. All simulations are run using CST MWS 2014 tool on system with Intel Xeon E5 2620 CPU and 16 GB RAM.

4.1. Analysis of antenna efficiency

First, we simulate and analyze antenna characteristics in intra chip environments using the three configurations described in previous section. The efficiency of integrated antennas in intra chip environments is degraded due to proximity of antennas to the metal layers. To improve the efficiency of antenna, we propose to place the antenna over a cavity region formed in between the interconnect layer, as shown in Fig. 1. The size of cavity in *X-Z* plane is determined by the antenna dimensions. The length of the cavity in X(Z) dimension is set to be 100 μm plus the longest dimension of the antenna in X(Z) dimension. We study return loss characteristics to analyze impact of metal interconnects on antenna bandwidth. Fig. 3 shows the return loss of PLPA and folded dipole antennas for different configurations. The dimensions of antennas in all three configurations are same; only the port impedance of the feed is adjusted in three cases to achieve reasonable return loss values. In No Metal Interconnects configuration, PLPA and folded dipole antennas have bandwidth of 1.5 GHz and 2 GHz respectively. When these antennas are placed in practical setup of intra chip environments (Antenna over Metal Region configuration), the bandwidth in both cases reduces; 1.16 GHz for PLPA antenna and 1 GHz for folded dipole antenna. By using dielectric filled cavity where antenna is etched, bandwidth of PLPA is 3.2 GHz and folded dipole is 2.4 GHz at their respective resonating frequencies. As can be observed from Fig. 3, the bandwidth improves by more than 100% while using Antenna over Cavity Region configuration for both antennas. Next, we compare the radiation efficiency of the antennas to observe the impact of metal interconnects.

The simulated efficiency of PLPA and folded dipole antennas, when placed in Antenna over Metal Region configuration, is 61.97% and 60.87% respectively. With *Antenna over Cavity Region* configuration, the efficiency increases to 94.11% at 58 GHz for PLPA and 93.45% at 59.61 GHz for folded dipole antennas. We have also verified, if using a top dielectric layer of higher thickness can improve the antenna efficiency in *Antenna over Metal Region* configuration. Even with increasing the thickness of top dielectric layer from 10 μm to 30 μm, the efficiency is increased only by five percentage points. Antenna over Cavity Region provides 1.5 the efficiency of that of existing configuration of metal layers inside the chip for both the antennas. Both radiation efficiency and bandwidth improve significantly when antennas are placed over cavity region, which is completely filled with SiO2 material as compared to existing setups, irrespective of antenna structure. For the remainder of results, we use Antenna over Cavity Region configuration, unless specified.

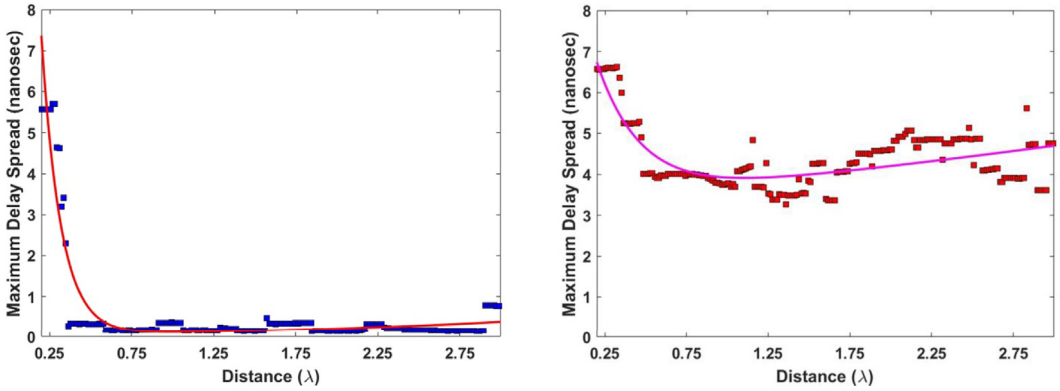
4.2. On-chip wireless channel

In this section, we study the properties of on-chip wireless channel and how the chip geometry impacts its characteristics. We derive the path loss, delay spread, propagation delay and their inter-dependencies as functions of transmitter-receiver distance.

4.2.1. Path loss estimation

The path loss of wireless channel determines the power requirements for reliably transmitting and receiving data using wireless communication. Intra chip environment with near field and multipath propagation effects degrades the performance of on-chip wireless channel. Fig. 4 shows variation of path loss in on-chip wireless channel with distance from transmitting antenna (represented in terms of wavelength) for both PLPA and folded dipole antennas. The field strength decay, unlike in far field region, does not vary as Friis transmission equation with distance from transmitting antenna. To measure path loss in near field region, we analyze the field at receiving antenna for different distances. Due to multipath propagation, signal components that reach the receiver include line-of-sight component, reflection from bottom layers and reflections from chip edges. The propagation components from reflections off of different layers and chip boundaries can interfere constructively/destructively depending upon distance from transmitting antenna.

The variation of field strength with distance can be divided into three distinct regions depending upon distance from antenna as shown in



(a) Planar Log Periodic Antenna (PLPA) (b) On-Chip Folded Dipole Antenna

Fig. 5. Variation of delay spread with distance from transmitting antenna.

Fig. 4. At distances very close to antenna (R1), signal decays at a moderate rate. In R2, with distance upto one-third of wavelength, there is high decay rate in signal strength. Finally, as distance from antenna increases beyond half wavelength (R3), decay rate becomes slower. For PLPA antenna in Fig. 4a, decay rates for three regions are 19dB/λ, 57dB/λ and 9dB/λ respectively. Similarly, for folded dipole from Fig. 4b, the values are 16dB/λ, 27dB/λ and 4dB/λ respectively. Path loss variation of folded dipole is significantly better than that of PLPA, which is due to higher number of multipath components with former. Omnidirectional antennas like folded dipole radiate in all directions, resulting in many reflected components from all chip edges. These components interfere at the receiver, improving the signal strength. On the other hand, directional antennas result in fewer reflection components as they radiate only in particular direction. Directional antennas, only when placed near chip boundaries experience significant impact from edge reflections. Hence, path loss variation in intra chip wireless channel depends on relative positions of antennas in X-Z plane and antenna radiation beamwidth along with channel characteristics. This requires that transmission power at any source needs to be adjusted depending upon receiver position or all transceivers need to be calibrated to worst case path loss. This either increases complexity of design or results in higher power requirements. A possible and efficient way to minimize the impact of this higher power consumption without increasing design complexity is to use low power design techniques like power gating for wireless interconnects [20,21].

4.2.2. Delay spread estimation

Another implication of complex chip geometries is time dispersion due to multiple paths and phase distortions caused by it. Delay spread gives the statistical measure of time dispersion nature of channel and is caused by signals from different propagating paths experiencing different propagation delays. As noted before, presence of different dielectric regions (Si substrate, SiO_2), multiple metal layer stack and chip boundaries lead to many propagation paths in on-chip wireless channel. This leads to many signal peaks and high delay spread. Maximum delay spread is calculated as difference of last and first-time instances of signal paths with strength above a threshold and its variation with transmission distance is shown in Fig. 5. We set the threshold as 40 dB below transmitted signal power, taking signal loss and noise sources inside the chip into consideration. The directionality and relative positions of antennas impact delay spread of the channel significantly.

As can be seen from Fig. 5a, delay spread for PLPA antenna presents an exponentially decreasing trend with increase in distance from the antenna. This can be understood from (a) the number of reflections from chip edges are less for PLPA as it is directional, thereby leading to smaller delay spread; (b) the thickness of different layers along Y-dimension is considerably smaller than transmission distance. Consequently, the path distance of different reflected components from different layers is similar and they experience almost equal delay. This results in reduced delay

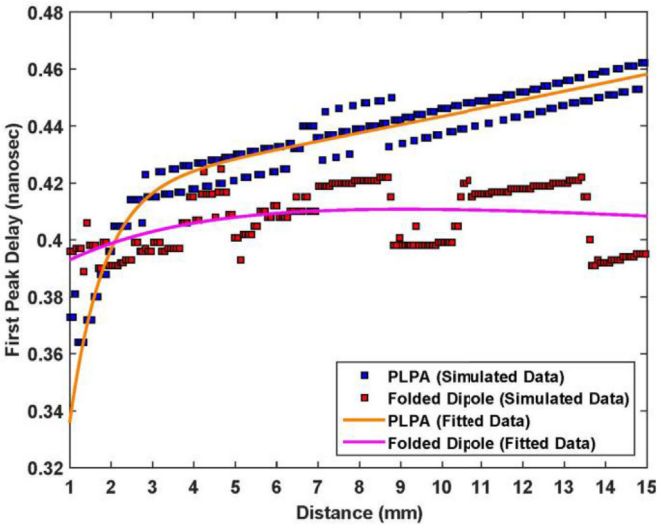


Fig. 6. Variation of propagation delay with transmission distance.

spread for directional antennas as transmission distance increases. For distances beyond λ, the delay spread is zero as observed from Fig. 5a. In case of folded dipole antenna from Fig. 5b, delay spread remains high even as distance increases. The high delay spread in folded dipole antenna is due to its omnidirectional nature. Just like with directional antenna, reflections from bottom layers converge. But, signal from omnidirectional antenna radiates in all directions, leading to larger number of reflections from all chip edges. The paths traveled by these multipath components vary significantly and hence they reach receiver with different propagation delays. This causes the delay spread to be much higher even at longer distances for omnidirectional antenna. Even at distances of 3λ, the delay spread is above 3nanosec from Fig. 5b.

4.2.3. Propagation delay estimation

The primary use of wireless transmission for intra chip communications is to reduce communication delay over long distances and overcome the challenges of traditional wired interconnects. We study delay characteristics of on-chip wireless channel with transmission distance. The variation of propagation delay with distance is presented in Fig. 6. The delay shows an exponential relation with transmission distance and becomes constant as distance increases. The delay varies significantly from free space de-lay and varies between 0.36 nanosec and 0.46 nanosec over distances upto 15 mm. In on-chip wireless channel, when source and receiver are far apart, the line-of-sight component interferes destructively with equally strong reflection from the interface of free space and

top dielectric layers. As a result, the line-of-sight component contributes negligibly to the received signal. Signal components propagating through and reflections from different layers dominate the received signal resulting in higher delay. Though delay in on-chip wireless channel is higher than free space delay, it is considerably better than that of long on-chip metal wires. At 15 mm distance, delay in long buffered and unbuffered wires is 0.9nanosec and 2.4nanosec [22] respectively as compared to 0.45nanosec for wireless.

5. On-chip wireless link design guidelines

The analysis of wireless channel in on-chip environment shows great deviation from free space channel, previously considered for WNoC evaluations. The intra chip wireless channel characteristics have to be into account for design of transceiver circuit components, wireless network, antennas and their placement and for WNoC performance evaluation. Based on the findings from the intra chip wireless channel analysis, we propose guidelines for WNoC design at all levels from manufacturing, circuit to system design.

1. Any metal lines in the proximity of the antennas, both in the same layer and layers below, must be avoided. An offset of at least 100 μm within the same layer is preferred for all other metal lines.
2. Cavity regions filled with dielectric material in the metal layer stack below antenna structures improve its bandwidth and radiation efficiency. Dielectric materials, besides SiO_2 may further improve performance and require detailed analysis.
3. Multi-carrier modulation schemes like OFDM are suitable for on-chip wireless communication due to resilience against high dispersion and multipath effects prevalent in intra chip wireless channel.
4. A trade-off exists between path loss, channel dispersion, broadcast capability in design of the wireless network.
5. Prudent network design using directional antennas that can establish communication between subsets of wireless nodes may provide robustness against high dispersion.
6. WNoCs, that strictly require broadcast capability between all wireless nodes, can use omnidirectional antennas with bandpass filters on the receiver side to account for dispersion.
7. Irrespective of the choice of antennas, power amplifier specifications must account for transmission power and path loss requirements. While, omnidirectional antennas exhibit better path loss variation, high performance and power overheads may exist for recovering time dispersed signal.
8. The higher power requirements highlight the need for more aggressive power saving techniques, akin to those in Refs. [20,21] for wireless transmission and transceivers.
9. High propagation delay and delay dispersion increase the overall channel access time for any single wireless transmission in the network. To ensure reliable transmission in any wireless network design, efficient and dynamic channel resource management techniques are required.
10. The adverse channel effects may require error detection or correction techniques in WNoCs. A detailed analysis of the reliability of on-chip wireless links, including error rate, channel capacity, etc. using end-to-end modelling of wireless communication is needed.

As highlighted by the design guidelines, the effects of wireless channel impact every aspect of system design, increasing the need for robust circuit and network design to ensure efficient and reliable WNoCs. Especially, system level studies must ensure incorporation of all these analyses and guidelines for both design and evaluation of WNoCs. In the next section, we provide a brief analysis of wireless link and network performance with free space channel assumption and intra chip channel characteristics.

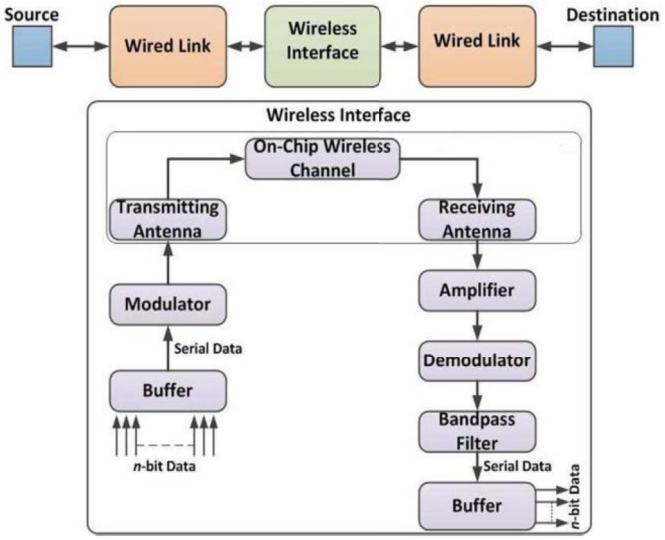


Fig. 7. A Typical Communication Path using Wireless Interfaces with all Components in NoC.

Table 3
Comparison between wired, free space wireless and intra chip wireless links.

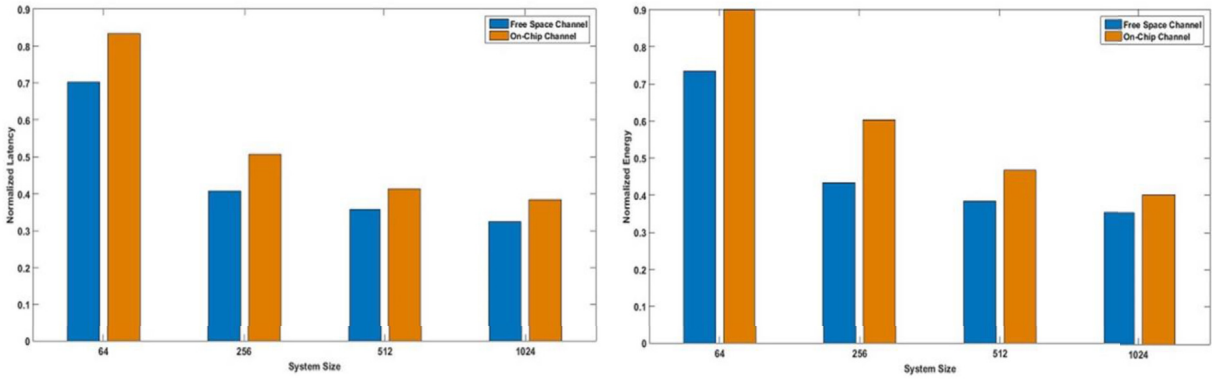
Metric	Wired	Free Space wireless	Intra Chip Wireless
Latency (picosec)	1159.3	33.33	473.5
Energy (pJ/bit)	18.2517	0.612	4.575

6. Impact on wireless interconnect performance

In this section, we briefly study the performance of wireless interconnects with free space and intra chip wireless channel. Data transmission using wireless links typically involves data conversion between digital and analog, modulation/demodulation, amplification and signal transmission through wireless channel. Different modules associated with wireless communication are shown in Fig. 7. Serializer/Deserializer (SERDES) buffers at the interface of WI converts data between n-bit parallel form and serial data stream. The serial data stream at transmitter is modulated and amplified before feeding into the antenna for transmission. We have used On-Off Keying (OOK) modulation scheme adopted from Ref. [23] for this evaluation. The received signal at the receiver is amplified and demodulated before converting back to parallel data. We find link latency and energy consumption using on-chip wireless channel and compare the values with that of wireless link using free space channel and wired links.

6.1. Interconnect latency

The packet latency while transmitting data using wireless links depends on SERDES delay, serial bit stream frequency and filtering delay along with the propagation delay of wireless channel. Table 3 shows the latency and energy values of buffered wired, free space wireless and intra chip wireless links at 20 mm distance between source and destination nodes. The propagation delay in on-chip wireless channel is ≈ 473.5picosec using directional antennas. The propagation delay with omnidirectional antennas is further lower than that with directional antennas. In comparison, propagation delay for free space wireless channel link, long unbuffered and buffered wired links is 33.33picosec, 3860.2picosec and 1159.3picosec respectively. While latency using wireless links is significantly better than wired links, it can be noted that packet latency in WNoCs is tenfold higher as compared to that of free space channel. The high propagation delay increases the active time and channel access time for each transmission, leading to higher energy



(a) Average Network Latency (b) Average Packet Energy

Fig. 8. Comparison of network performance with on-chip and free space wireless communication models.

consumption and challenges for efficient management of shared channel among all wireless nodes.

Additionally, channel delay dispersion further increases overall packet latency to receive all signal components at the receiver. Especially, omnidirectional links have dispersion running into several nanosec. Combining propagation delay and delay spread along with other circuit delays, the worst case latency with directional and omnidirectional antennas is 550picosec and 3400picosec (without any compensation) respectively. While directional links perform 85.75% and 52.56% better, omnidirectional links perform the same as compared to long unbuffered and buffered wired links. Considering wired link layout issues and transfer through multiple layers, on-chip wireless links provide significant benefits at long distances. However, data transmission latency with delay dispersion runs into several system clock cycles and needs to be accounted for designing and evaluating WNoCs.

6.2. Energy consumption

The energy per bit for an interconnect gives a measure of energy expended in transmitting a bit and is the total sum of power dissipated in all wireless components for the entire duration of the transmission. All the OOK based transceiver components consume 32 mW of power. At 20 mm distance, path loss in on-chip wireless channel for directional and omnidirectional antennas is 39 dB and 29 dB respectively. Furthermore, omnidirectional links require high frequency bandpass filters [24] to compensate for high delay spread, which increases overall loss to 34 dB. Considering all losses and power requirements, on-chip wireless links consume 4.575pJ/bit (for directional antenna) to transmit data over 20 mm distance, as opposed to 0.612pJ/bit, assuming free space channel. The transceiver design, especially in terms of transmission power requirements needs to consider the higher path loss of on-chip wireless links. In comparison, long wired links consume 18.2517pJ/bit and 82.0257pJ/bit energy at 20 mm distance for buffered and unbuffered respectively [22]. In addition, energy consumption for wired links increases exponentially with distance, while wireless link energy increases linearly providing high energy savings for long distances across the chip.

6.3. Network performance

The analysis of link latency and energy consumption provides an understanding of how on-chip wireless links perform as compared to free space channel and long wired links. We utilize this to measure the network performance with intra chip channel characteristics. For network level evaluation, we compare the performance and energy consumption of WNoC topology with a baseline wired mesh topology. The topologies of baseline wired mesh and WNoC are adopted from Ref. [1]. The entire system is divided into multiple clusters; with all nodes in a cluster interconnected using a star topology to a hub and all hubs arranged in mesh topology. WNoC further augments the wired mesh network with mm-wave, long range wireless links. The number of wireless links at different system sizes is 3, 7, 10 and 14 for 64, 256, 512 and 1024 cores respectively. WNoC topology is evaluated with both free space and intra chip wireless channel characteristics.

Fig. 8 shows normalized packet latency and energy under uniform random traffic for different system sizes with wireless links for both free space and on-chip channel cases. The latency and energy values are normalized by corresponding values of baseline wired mesh topology of same system size.

As observed from Fig. 8, WNoC performs better than wired only mesh topology, but the amount of improvement attained is slightly lower as compared with that of free space assumption. The average packet latency with on-chip wireless links is higher by 15% 25% than that of free space wireless links for different system sizes. For a system with 256 cores, WNoC provides 50.72% improvement in latency as opposed to 60% when free space channel is considered. In terms of packet energy, WNoC with on-chip wireless links offers little savings at smaller system sizes, unlike WNoC with free space channel assumption. For a 256-core system, WNoC saves 40% energy over wired mesh and the energy savings become more significant as system size increases further. This can be observed from the fact that, with increasing number of cores, distance between nodes increases and benefits of wireless links become more apparent. The energy savings can be further improved by use of power gating for transceiver circuits. The analysis of network performance at different system sizes shows that, though performance of on-chip wireless links is lower than free space links, WNoC offers considerable savings in latency and energy for many core architectures.

6. Conclusion

This work presents a comprehensive analysis of intra chip wireless channel and its impact on wireless NoC design using 3D model that captures key chip components influencing wireless transmission. Design guidelines for antenna choice and implementation are provided to improve performance. Radiation efficiency and antenna bandwidth are greatly improved by placing antenna over a dielectric filled cavity. Analysis show that propagation in on-chip wireless channel is predominantly in near field/transition region, making channel more complex. Path loss and delay spread of the channel have been analyzed and their inter-dependencies have been studied. Directional antennas are less effected by channel time dispersion but exhibit higher losses and vice-versa for omnidirectional antennas. A trade-off between loss and time dispersion needs to be made based on network requirements. A brief illustration of wireless performance shows that intra chip channel limits achieved network performance and impacts circuit design in terms of power and control hardware. The on-chip wireless channel estimation provides insight into characteristics of wireless links and provides means

for circuit designers to better tune specifications for achieving required performance.

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